



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/739,200	12/19/2003	Masao Okihara	OKI.602	9880

7590 05/25/2004
VOLENTINE FRANCOS, PLLC
Suite 150
12200 Sunrise Vally Drive
Reston, VA 20191

EXAMINER

THAI, LUAN C

ART UNIT PAPER NUMBER

2827

DATE MAILED: 05/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AY

Office Action Summary

Applicati n N

10/739,200

Applicant(s)

OKIHARA, MASAO

Examiner

Luan Thai

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on _____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3 and 4 is/are rejected.
- 7) ☒ Claim(s) 2,5 and 6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>12/19/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The Information disclosure Statement filed on 12/19/03 has been considered.

Drawings

3. Figure 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1 and 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art (Fig. 8 hereinafter "Fig. 8") in view of Dennison et al (6,537,891).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1 and 3-4, the prior art of "Fig. 8" discloses a variable threshold voltage complementary MOSFET with a SOI structure, combined a N-channel MOSFET with a P-channel MOSFET, comprising: a SOI substrate main body having a support substrate (10), an insulating layer (20) disposed on the support substrate, and island-shaped first layer (31-33-35) and second silicon layers (37-39-42) separately formed on the insulating layer (20); a first MOSFET (12) formed of a fully depleted SOI where a first channel part is formed in the first silicon layer (31-33-35); a second MOSFET (14) formed of a fully depleted SOI where a second channel part is formed in the second silicon layer (37-39-42), the second MOSFET configuring a complementary MOSFET with the first MOSFET; and an adjusted bias electrode (63) disposed on the support substrate (10) for applying an adjusted bias voltage to adjust threshold voltage of the complementary MOSFET to the SOI substrate main body. The structure of "Fig. 8" described above shows both MOSFETs (12/14) being formed of fully depleted SOI; and thus, it fails to disclose one MOSFET being formed of a *fully depleted SOI* and another MOSFET being formed of a *partially depleted SOI*.

Dennison et al while related to a similar variable threshold voltage complementary with a SOI design teach a SOI device comprising not only a fully depleted structure but also a partially depleted structure (Col. 2, lines 5+, Col. 3, lines 50+) in order to have a higher drive current through the channel region, which will allow for faster operation of the integrated circuit (Col. 1, lines 53+). It would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the device structure shown in the prior art of "Fig. 8" by forming one MOSFET of a fully depleted SOI and another MOSFET of partially depleted SOI, as taught by Dennison et al., for the purpose of having a higher drive current through the channel region, which will allow for faster operation of the integrated circuit.

Allowable Subject Matter

6. Claims 2 and 5-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
7. The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken either singly or in combination fails to anticipate or fairly suggest: a neutral region for suppressing adjusting threshold voltage of the second MOSFET by the adjusted bias voltage, and a suppressed voltage electrode disposed so as to contact with the neutral region for applying suppressed voltage to suppress the threshold voltage to the neutral region, as recited in claim 2; especially when these limitations are considered within the specific combination claimed.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935.

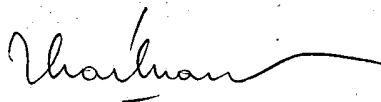
The examiner can normally be reached on 6:45 AM - 4:15 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Luan Thai

May 20, 2004

United States Patent & Trademark Office

Primary Examiner

Jef-6A15

Art Unit 2827

(571) 272-1935